SAN DIEGO STATE UNIVERSITY STUDENT CLUSTER COMPETITION TEAM

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Bit Benders

ABSTRACT

The San Diego State University Student Cluster Competition (SCC) team is participating in the SCC16 for the first time [1]. The cluster (provided by Intel, who is our project sponsor) is based on 8 Kennedy Pass processors, for a total of 320 cores. In this competition, the team has learned: cluster assembly and administration, parallel programming; and how to profile 5 different HPC applications. The outcome of these activities have enhanced the students' experiences of using HPC and motivated them to solve complex problems using advanced HPC skills and facilities.

ABOUT THE BIT BENDERS TEAM

Our team has depth, strength. diversity, and a sense of fun:

- **Student Team:** are volunteers who have shown the ability to be successful undergraduates students at SDSU. Most have done some type of HPC/parallel computing on their own, or through internships or online courses. Team members are:
  - Ali Esparza, Senior (CS), HPCG
  - Tuan Nugyen, Senior (CS), ParConnect
  - Vaughn Ganem Haka, Senior (Eng), Password cracking
  - Armando Ramos, Sophomore (CS), Power outage/admin
  - Gary Williams, Senior (CS), HPL, admin
  - Briana Wright, Senior (CS), ParaView, architecture
- **Faculty mentors:** several SDSU faculty have helped with our efforts, including:
  - Dr. James Otto (CSRC);
  - Dr. Chris Paolini (Engineering);
  - Dr. Peter Blomgren (Math);
  - Dr. Jose Castillo (Director, CSRC).
- **Vendor partners:** our partners have been committed to working with the team, which helped ensure that the software and hardware used is dependable and useful for the SCC challenge. In particular,
  - Reese Baird (Intel, OpenHPC)
  - Dr. Pietro Cicotti (San Diego Supercomputer Center).
- The name of the team arose from a common love of Futurama, and the connection that we could bend computer bits to our will, hence the name "Bit Benders." Our tag line is "Byte our shiny metal hash."
- : Visit our Web page: **http://www.csrc.sdsu.edu/sc/sc16/scc/**

TEAM PREPARATION

To prepare for the SCC competition, the team met throughout the Summer focusing on key HPC topics, including:

- Introduction to MPI
- Studied one application each week.
- Profiling, scaling, performance monitoring and run-time code profiling (using tools such as gprof, MPI timers, and Allinea DDT).
- OpenHPC software stack - learning which components will work best for each app and why.

In addition to learning about the software, the team helped to build the cluster:

- cluster design and and network interconnection;
- building the rack and installing servers and switches;
- installing memory, SSD drives, IB cards, etc.;
- connecting ethernet and infiniband networks.

ACKNOWLEDGEMENTS

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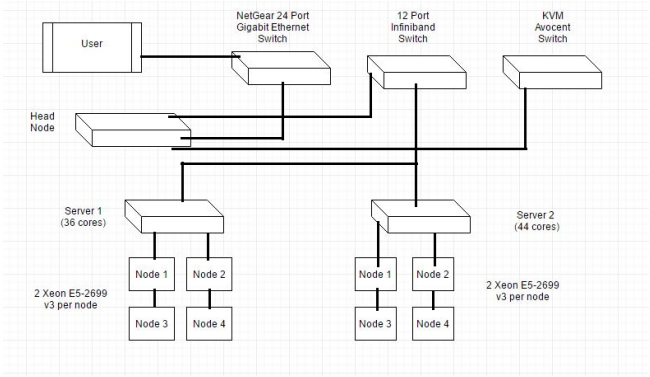
REFERENCES

[1] Supercomputing '16 Student Cluster Competition. Last Accessed on 11/1/16 at http://www.studentclustercompetition.us/.

[2] Detailed Specifications of the Intel Xeon E5-2600v4 "Broadwell-EP" Processors. Last Accessed on 11/01/16 at https://www.microway.com/knowledge-center-articles/detailed-specifications-of-the-intel-xeon-e5-2600v4-broadwell-ep-processors/.



THE NIBBLER CLUSTER ARCHITECTURE

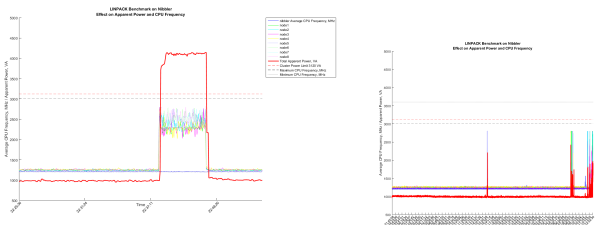
- **Head node:** Intel Xeon DP Broadwell-EP E5-2680 28 core server used for login access, system management, queuing, systems, display monitor, etc.
- **Compute nodes:** Two Kennedy Pass Intel Quad board Servers [2], for a combined total of 320 cores and nominal peak performance of approximately 7-8 TFlops.
- **Networking and Connectivity:** The system uses both GigE and Infiniband networks. The Ethernet network is managed by a 24 port router, and is used as a LAN, for managing the cluster and allowing users to access the system via laptops. The IB interconnection network connects the compute nodes together and is used for computational work.
- **Rack:** all the hardware, including the interconnect fabric, fits into an open sided 42U rack.
- **Performance:** Theoretical peak performance is appx. 11.5 TFlops for 320 cores.
- **Power Usage:** Power benchmark tests have shown that the cluster, when running the HPL benchmark at full capacity, is above the 3.1 KW limit of the competition. We plan to run the benchmark and turn off 1 or 2 nodes as required during the qualification process.

APPLICATION STRATEGIES

We have developed strategies for running and optimizing the applications, including:

- Participate in Saturday lab meetings to promote team discussion and interactions.
- Assign a team lead for each application.
- Working with faculty mentors to choose right compilers and environments;
- Profiling applications for optimization.
- Create an application profile/prediction summaries.
- Develop scripts and analysis tools for run time control and data display including a power usage monitoring script and a script to turn cores on/off for each node.

FIGURE 1



The power monitoring scripts show the outputs of the apparent power usage for each node, using SNMP queries to the Geist PDU. The plots also show the CPU clock speed for every core, obtained from /proc/cpuinfo. The figures above show the the power consument when running the HPL benchmark on the full system of 320 cores (left), and on a smaller system of 220 cores (right). For the case of 320 cores, the power usage exceeds the power limit of 3.1 KW, but stays under the limit when the number of active cores is reduced to 220.